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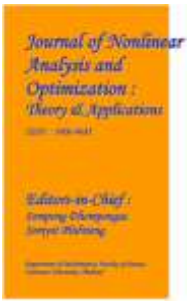

Architectural design of Shift Registers using Pulsed Latches

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Abstract:The power consumption and area reduction are the key challenges in the Very Large Scale Integration (VLSI) circuit design. The shift register is the main building block in the VLSI circuits. The shift register is composed of clock interconnection network and timing elements such as flip-flops and latches this clock entomb association system and timing component is the primary power and region expending component in the move enlist. This clock interconnection network and timing element is the main power and area consuming element in the shift register. This project introduces a low power and area efficient shift register using pulsed latch and pulse generation circuit. The area and power consumption will be reduced to 50%in the shift register if the Flip-Flop is replaced with the pulsed latch. This technique explains the timing problem between pulsed latches through the use of multiple nonoverlap delayed pulsed clock signals as an alternative of the conventional single pulsed clock signal.

I. INTRODUCTION

A Shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [1], communication receivers [2], and image processing ICs [3]–[5]. Recently, as the size of the image data continues to increase due to the high demand for high quality image data, the word length of the shifter register increases to process large image data in image processing ICs. An image-extraction and vector generation VLSI chip uses a 4K-bit shift register [3]. A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [4]. A 16-megapixel CMOS image sensor uses a 45K-bit shift register [5]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

The architecture of a shift register is quite simple. An N-bit shift register is composed of series connected N data flip-flops. The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. This paper proposes a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches.

II. Literature Survey

An arrayed-shift-register architecture has been employed in conjunction with a pipelined directional-edge-filtering circuitry. As a result, it

has become possible to scan an image, pixel by pixel, with a 64 x 64-pixel recognition window and generate a 64-dimensional feature vector in every 64 clock cycles. In order to determine the threshold for edge-filtering operation adaptive to local luminance variation, a high-speed median circuit has been developed. A binary median search algorithm has been implemented using high-precision majority voting circuits working in the mixed-signal principle. A prototype chip was designed and fabricated in a 0.18-mum 5-metal CMOS technology. A high-speed feature vector generation in less than 9.7 ns/vector element has been experimentally demonstrated. It is possible to scan a VGA-size image at a rate of 6.1 frames/s, thus generating as many as 1.5×10^6 feature vectors per second for recognition. This is more than 10^3 times faster than software processing running on a 3-GHz general-purpose processor.

This paper presents a 10-bit column driver IC for active-matrix LCDs, with a proposed iterative charge-sharing based (ICSB) capacitor-string that interpolates two output voltages from a resistor-string DAC. Iterative mode change between a capacitive voltage division mode and a charge sharing mode in the ICSB capacitor-string interpolation suppresses the effect of mismatches between capacitors and that of parasitic capacitances; thus, a highly linear capacitor sub-DAC is realized. In addition, the area-sharing layout technique, which stacks the interpolation capacitor-string on top of the R-DAC area, reduces the driver channel size and extends the bit resolution of the gamma-corrected nonlinear main R-DAC. Consequently, the proposed ICSB capacitor-string interpolation scheme provides highly uniform channel performance by passively dividing the coarse voltages from the global resistor-string DAC with high area efficiency, and more effective bit resolution for nonlinear gamma correction.

III. Existing System

Shift Registers: The Shift Register is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name shift register. It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. The data bits may be fed in or out of the register serially, i.e. one after the other from either the left or the right direction, or in parallel, i.e. all together. The number of individual data latches required to make up a single Shift Register is determined by the number of bits to be stored with the most common being 8-bits wide, i.e. eight individual data latches. Shift Registers are used for data storage or data movement and are used in calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

• Serial-in to Parallel-out (SIPO) - The register is loaded with serial data, one bit at a time, with the stored data being available in parallel form

• Serial-in to Serial-out (SISO) - The data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.

• Parallel-in to Serial-out (PISO) - The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.

• Parallel-in to Parallel-out (PIPO) - The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse. The effect of data movement from left to right through a shift register can be presented graphically.

IV Proposed System

An N-bit shift register is composed of series connected N data flip-flops.The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flips in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop [6]–[9]. But the pulsed latch cannot be used in

a shift register due to the timing problem between pulsed latches.

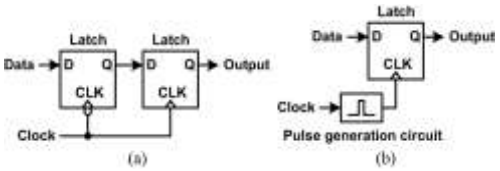


Figure-1: (a) Master-slave flip-flop (b) Pulsed latch

A master-slave flip-flop using two latches in Fig. 1(a) can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal in Fig. 1(b)[6]. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for small area and low power consumption.

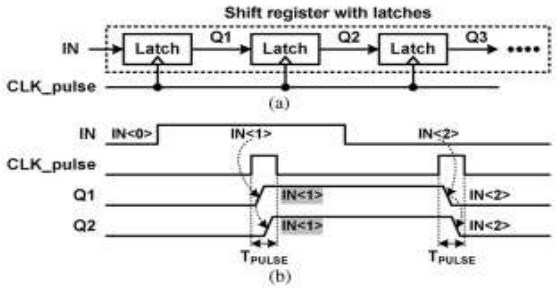


Figure 4.1: Shift register with latches and a pulsed clock signal. (a) Schematic. (b)Waveforms.

The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 3.1. The shift register in Fig. 4.1(a) consists of several latches and a pulsed clock signal (CLK_pulse). The operation waveforms in Fig. 4.1(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the input signal of the first latch (IN) is constant during the clock pulse width (T_{PULSE}). But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

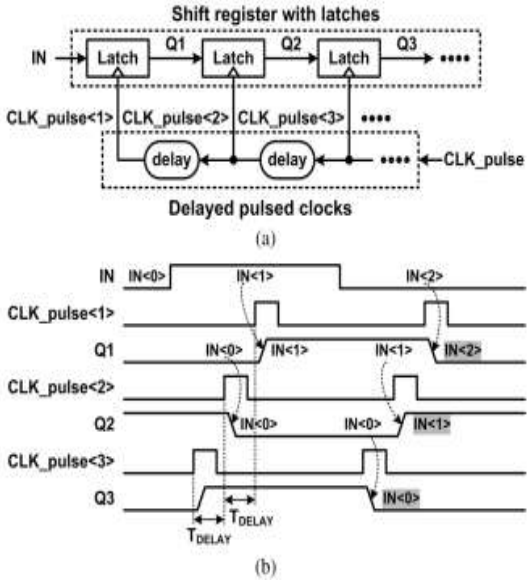


Figure 4.2: shift register with latches and pulsed clock signals (a) schematic (b) wave forms

However, the delay circuits cause large area and power overheads. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4.2(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches.

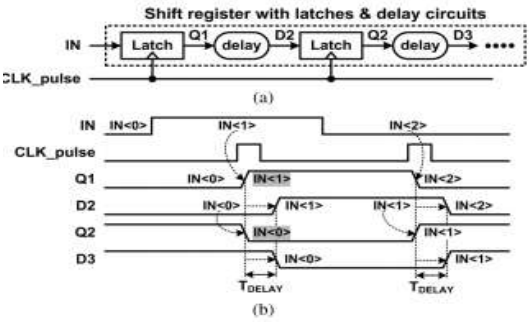


Figure.4.3: Shift register with latches, delay circuits, and a pulsed clock signal. (a) Schematic. (b) Waveforms.

One solution for the timing problem is to add delay circuits between latches, as shown in Fig. 4.3(a). The output signal of the latch is delayed and reaches the next latch after the clock pulse. As shown in Fig. 4.3(b). the output signals of the first and second latches (Q1 and Q2) change during the clock pulse width, but the input signals of the

second and third latches (D2 and D3) become the same as the output signals of the first and second latches (Q1 and Q2) after the clock pulse. As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches.

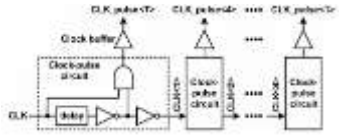


Figure 4.4: delayed pulsed clock generator

Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 4.4. The sequence of the pulsed clock signals is in the opposite order of the five latches. Initially, the pulsed clock signal CLK_pulse⟨T⟩ updates the latch data T1 from Q4. And then, the pulsed clock signals CLK_pulse⟨1:4⟩ update the four latch data from Q4 to Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

As shown in Fig. 4.4each pulsed clock signal is generated in a clock-pulse circuit consisting of a delay circuit and an AND gate. When an N-bit shift register is divided into K-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latches require K+1 pulsed clock signals. The number of sub shift registers (M) becomes N/K, each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches.

The conventional delayed pulsed clock circuits in Fig. 4.2 can be used to save the AND gates in the delayed pulsed clock generator in Fig.4.4 In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 4.4 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

The power is consumed mainly in latches and clock-pulse circuits. Each latch consumes power for data transition and clock loading. When the circuit powers are normalized with a latch, the power consumption of a latch and a clock-pulse circuit are 1 and α_P, respectively. The total power consumption is also $\alpha_P \times(K+1) +N(1+1/K)$. An integer for the minimum power is selected as a divisor of N, which is nearest to $\sqrt{(N/\alpha_P)}$. In K selection, the clock buffers in Fig. 3.4 are not considered. The total size of the clock buffers is determined by the total clock loading of latches. Although the number of latches increases from N to N(1+1/K) , the increment ratio of the clock buffers is small. The number of clock buffers is K. As K increases, the size of a clock buffer decreases in proportion to 1/K. because the number of latches connected to a clock buffer M= N/K is proportional to 1/K. Therefore, the total size of the clock buffers increases slightly with increasing K and the effect of the clock buffers can be neglected for choosing K.

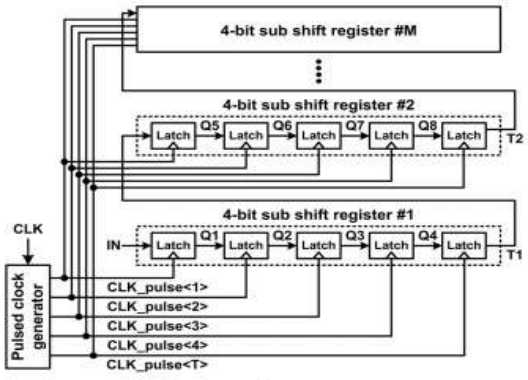


Figure 4.5: proposed shift register

However, this solution also requires many delay circuits. Fig. 4.5 shows an example theproposed shift registers. The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches, and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse⟨1:4⟩ and CLK_pulse⟨T⟩). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 4.5 (b) shows the operation waveforms in the proposed shift register.

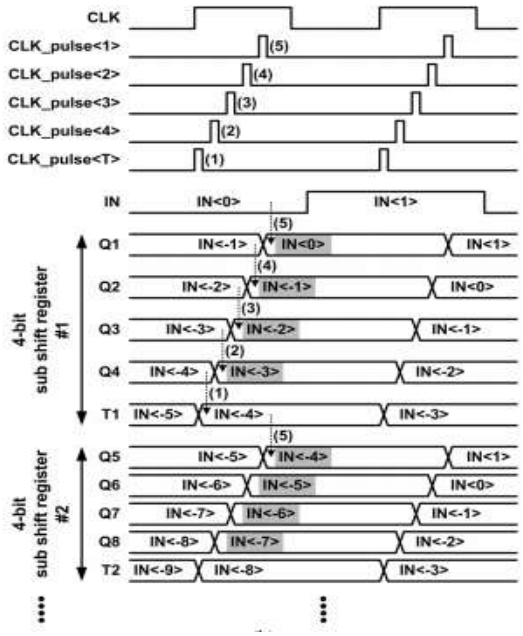
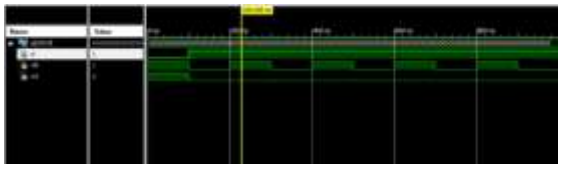


Figure 4.6: proposed shift registers wave forms

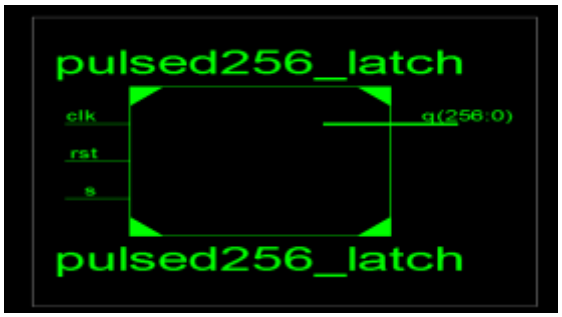
IV. Results

Result of the proposed design is implemented using Xilinx ISE for simulation and Synthesis.

Simulation.



Synthesis Result:



RTL Schematic

Design Summary.

Timing Summary.

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Timing Summary:
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Speed Grade: -2

   Minimum period: 1.069ns (Maximum Frequency: 935.454MHz)
   Minimum input arrival time before clock: 0.775ns
   Maximum output required time after clock: 0.880ns
   Maximum combinational path delay: No path found
```

V. CONCLUSION

This paper proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal. A small number of the pulsed clock signals is used by grouping the latches to several sub shifter registers and using additional temporary storage latches.

REFERENCES

[1] P. Reyes, P. Reviriego, J. A. Maestro, and O. Ruano, "New protection techniques against SEUs for moving average filters in a radiation environment," IEEE Trans. Nucl. Sci., vol. 54, no. 4, pp. 957–964, Aug. 2007.

[2] M. Hatamian et al., "Design considerations for gigabit ethernet 1000 base-T twisted pair transceivers," Proc. IEEE Custom Integr. Circuits Conf., pp. 335–342, 1998.

[3] H. Yamasaki and T. Shibata, "A real-time image-feature-extraction and vector-generation vlsi employing arrayed-shift-register architecture," IEEE J. Solid-State Circuits, vol. 42, no. 9, pp. 2046–2053, Sep. 2007.

[4] H.-S. Kim, J.-H. Yang, S.-H. Park, S.-T. Ryu, and G.-H. Cho, "A 10-bit column-driver IC with parasitic-insensitive iterative charge-sharing based capacitor-string interpolation for mobile active-matrix LCDs," IEEE J. Solid-State Circuits, vol. 49, no. 3, pp. 766–782, Mar. 2014.

[5] S.-H. W. Chiang and S. Kleinfelder, "Scaling and design of a 16-megapixel CMOS image sensor for electron microscopy," in Proc. IEEE Nucl. Sci. Symp. Conf. Record (NSS/MIC), 2009, pp. 1249–1256. [6] S. Heo, R. Krashinsky, and K. Asanovic, "Activity-sensitive flip-flop and latch selection for reduced energy," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 15, no. 9, pp. 1060–1064, Sep. 2007.

[7] S. Naffziger and G. Hammond, "The implementation of the nextgeneration 64 b itanium microprocessor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2002, pp. 276–504.

[8] H. Partovi et al., "Flow-through latch and edge-triggered flip-flop hybrid elements," IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 138–139, Feb. 1996.

[9] E. Consoli, M. Alioto, G. Palumbo, and J. Rabaey, "Conditional push-pull pulsed latch with 726 fJops energy delay product in 65 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2012, pp. 482–483.

[10] V. Stojanovic and V. Oklobdzija, "Comparative analysis of masterslave latches and flip-flops for high-performance and

low-power systems," IEEE J. Solid-State Circuits, vol. 34, no. 4, pp. 536–548, Apr. 1999.

[11] J. Montanaro et al., "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," IEEE J. Solid-State Circuits, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[12] S. Nomura et al., "A 9.7 mW AAC-decoding, 620 mW H.264 720p 60fps decoding, 8-core media processor with embedded forwardbody-biasing and power-gating circuit in 65 nm CMOS technology," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2008, pp. 262–264. [13] Y. Ueda et al., "6.33 mW MPEG audio decoding on a multimedia processor," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2006, pp. 1636–1637.

[14] B.-S. Kong, S.-S. Kim, and Y.-H. Jun, "Conditional-capture flip-flop for statistical power reduction," IEEE J. Solid-State Circuits, vol. 36, pp. 1263–1271, Aug. 2001.

[15] C. K. Teh, T. Fujita, H. Hara, and M. Hamada, "A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40 nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, Feb. 2011, pp. 338–339